

CD74HCT4066-Q1 HIGH-SPEED CMOS LOGIC QUAD BILATERAL SWITCH

SCLS581B – APRIL 2004 – REVISED APRIL 2008

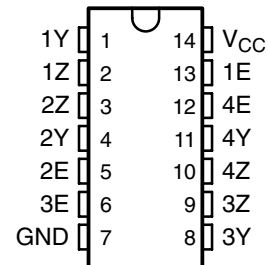
- Qualified for Automotive Applications
- Low ON Resistance
– 25 Ω Typical ($V_{CC} = 4.5\text{ V}$)
- Fast Switching and Propagation Speeds
- Low OFF Leakage Current
- Wide Operating Temperature Range: -40°C to 125°C
- Direct LSTTL Input Logic Compatibility:
 $V_{IL} = 0.8\text{ V Max}$, $V_{IH} = 2\text{ V Min}$
- CMOS Input Compatibility: $I_I \leq 1\ \mu\text{A}$ at V_{OL} , V_{OH}

description/ordering information

The CD74HCT4066 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operation speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

These switches feature the characteristic linear ON resistance of the metal-gate CD4066B. Each switch is turned on by a high-level voltage on its control input.

M OR PW PACKAGE
(TOP VIEW)



ORDERING INFORMATION†

T _A	PACKAGE‡		ORDERABLE PART NUMBER§	TOP-SIDE MARKING
	SOIC – M	Reel of 2500		
–40°C to 125°C	SOIC – M	Reel of 2500	CD74HCT4066QM96Q1	HCT4066Q
	TSSOP – PW	Reel of 2000	CD74HCT4066QPWRQ1	HK4066Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

§ The suffix 96 denotes tape and reel.

FUNCTION TABLE

INPUT nE	SWITCH
L	Off
H	On

H = High level

L = Low level



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 **TEXAS
INSTRUMENTS**

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
t _t	Input transition (rise and fall) time	V _{CC} = 4.5 V		0 500 ns
T _A	Operating free-air temperature	-40	125	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _I	V _{CC}	T _A = 25°C			T _A = -40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
I _{IL}	Any control	V _{CC} or GND	5.5 V			±0.1		±1	μA
I _{Iz}	V _{IS} = V _{CC} or GND	V _{IL}	5.5 V			±0.1		±1	μA
r _{on}	I _O = 1 mA, See Figure 7	V _{IS} = V _{CC} or GND	V _{CC}	4.5 V	25	80		128	Ω
		V _{IS} = V _{CC} to GND	V _{CC}	4.5 V		35	95		
Δr _{on}	Between any two switches	V _{CC}	4.5 V		1				Ω
I _{CC}		V _{CC} or GND	5.5 V			2		40	μA
ΔI _{CC}	Per input pin: 1 unit load, See Note 5	V _{CC} - 2.1 V	4.5 V to 5.5 V		100	360		490	μA
C _I	Control inputs					10		10	pF

NOTE 5: For dual-supply systems, theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT input loading

INPUT	UNIT LOADS†
All	1

† Unit load is ΔI_{CC} limit specified in the electrical characteristics table, e.g., 360 μA max at 25°C.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			T _A = -40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t _{pd}	Y or Z	Z or Y	C _L = 15 pF	5 V	4					ns
			C _L = 50 pF	4.5 V	12			18		
t _{en}	E	Y or Z	C _L = 15 pF	5 V	9					ns
			C _L = 50 pF	4.5 V	24			36		
t _{dis}	E	Y or Z	C _L = 15 pF	5 V	14					ns
			C _L = 50 pF	4.5 V	35			53		

operating characteristics, V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns

PARAMETER	TYP	UNIT
C _{pd} Power dissipation capacitance (see Note 6)	38	pF

NOTE 6: C_{pd} is used to determine the dynamic power consumption (P_D), per package.

$$P_D = (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma (C_L + C_S) \times V_{CC}^2 \times f_O$$

f_O = output frequency

f_I = input frequency

C_L = output load capacitance

C_S = switch capacitance

V_{CC} = supply voltage

analog channel characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC}	TYP	UNIT
f _{max} Switch frequency response bandwidth at -3 dB	See Figure 2 and Figure 8 and Notes 7 and 8	4.5 V	200	MHz
Crosstalk between any two switches	See Figure 1 and Figure 9 and Notes 8 and 9	4.5 V	-72	dB
Total harmonic distortion	See Figure 3, 1 kHz, V _{IS} = 4 V _{P-P}	4.5 V	0.023	%
Control to switch feedthrough noise	See Figure 4	4.5 V	130	mV
Switch OFF signal feedthrough	See Figure 5 and Figure 9 and Notes 8 and 9	4.5 V	-72	dB
C _S Switch input capacitance			5	pF

NOTES: 7. Adjust input voltage to obtain 0 dBm at output, f = 1 MHz.

8. V_{IS} is centered at V_{CC}/2.

9. Adjust input for 0 dBm at V_{IS}.



PARAMETER MEASUREMENT INFORMATION

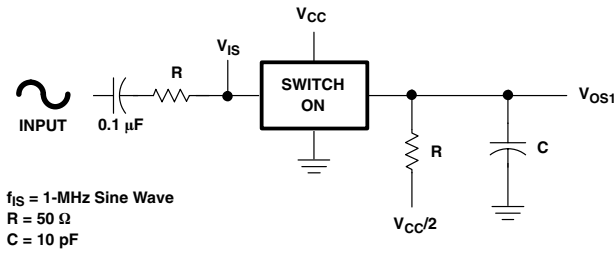


Figure 1. Crosstalk Between Two Switches Test Circuit

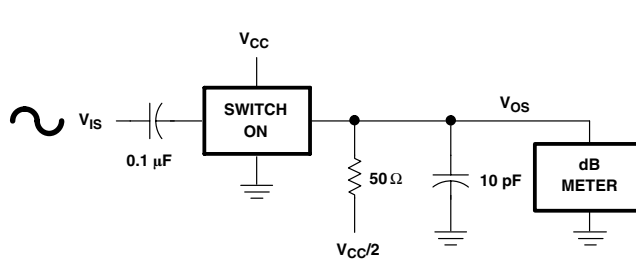
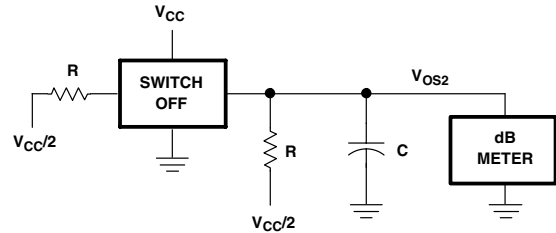


Figure 2. Frequency-Response Test Circuit

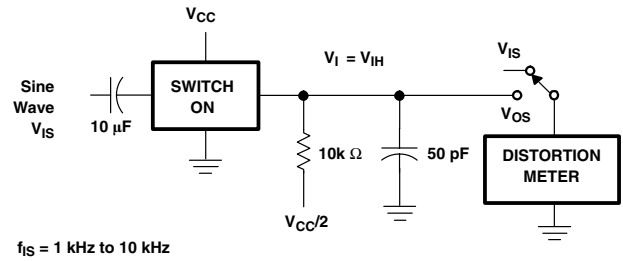


Figure 3. Total Harmonic Distortion Test Circuit

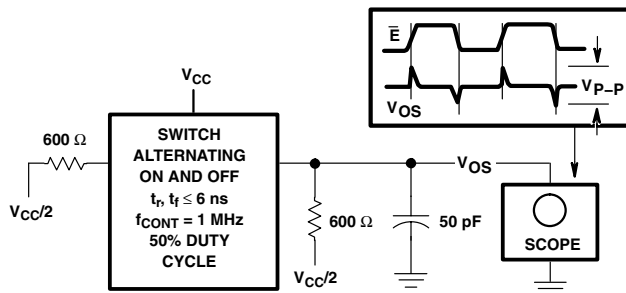


Figure 4. Control-to-Switch Feedthrough Noise Test Circuit

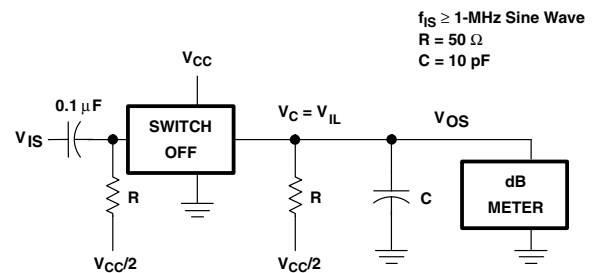
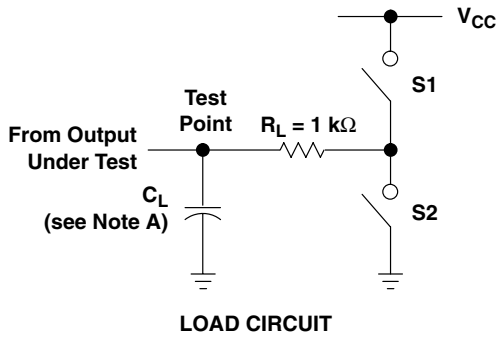
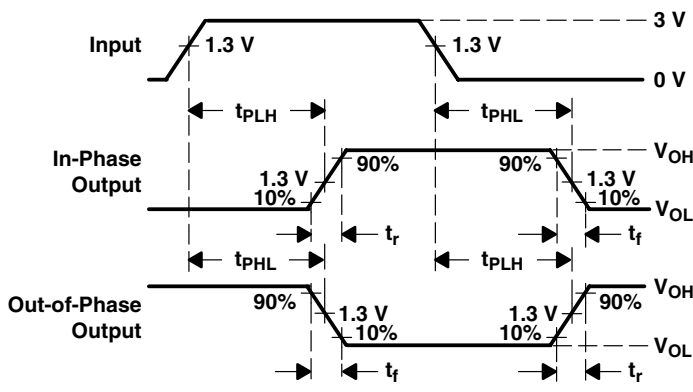


Figure 5. Switch OFF Signal Feedthrough Test Circuit

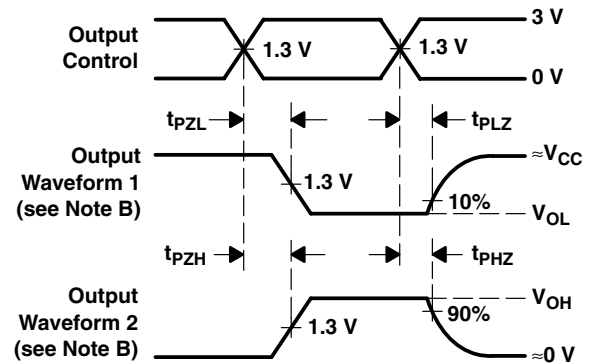
PARAMETER MEASUREMENT INFORMATION



PARAMETER		S1	S2
t_{en}	t_{pZH}	Open	Closed
	t_{pZL}	Closed	Open
t_{dis}	t_{pHZ}	Open	Closed
	t_{pLZ}	Closed	Open
t_{pd}		Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 E. The outputs are measured one at a time, with one input transition per measurement.
 F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 G. t_{PZL} and t_{PZH} are the same as t_{en} .
 H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 6. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

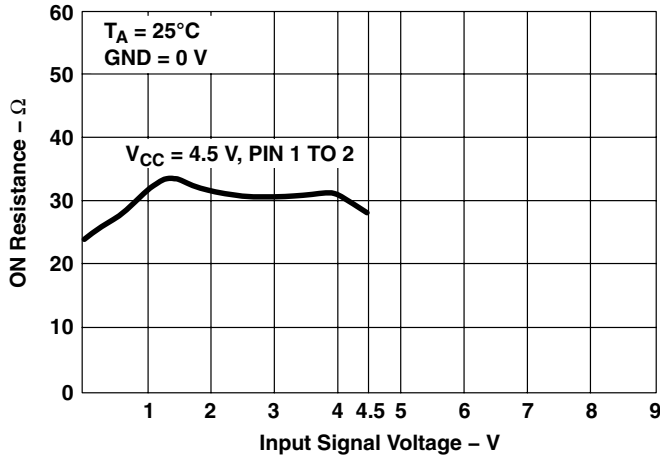


Figure 7. Typical ON Resistance vs Input Signal Voltage

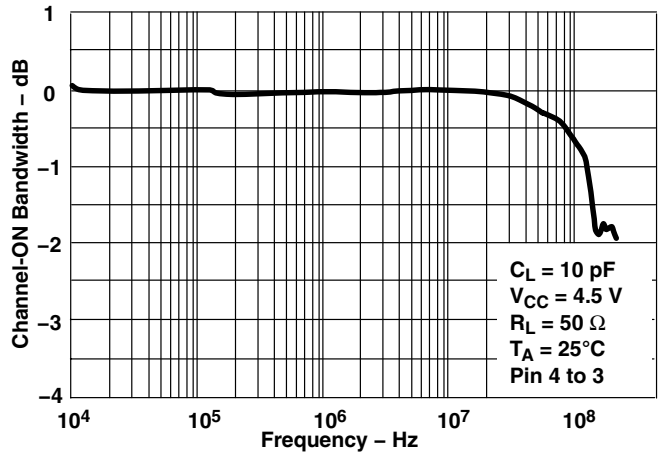


Figure 8. Switch Frequency Response, $V_{CC} = 4.5 \text{ V}$

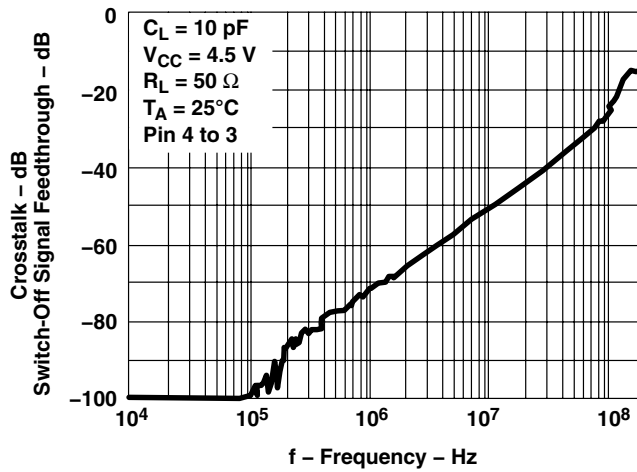


Figure 9. Switch-OFF Signal Feedthrough and Crosstalk vs Frequency, $V_{CC} = 4.5 \text{ V}$

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74HCT4066QM96Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4066QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
D24066QM96G4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
HCT4066QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD74HCT4066-Q1 :

- Catalog: [CD74HCT4066](#)



NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

D (R-PDSO-G14)

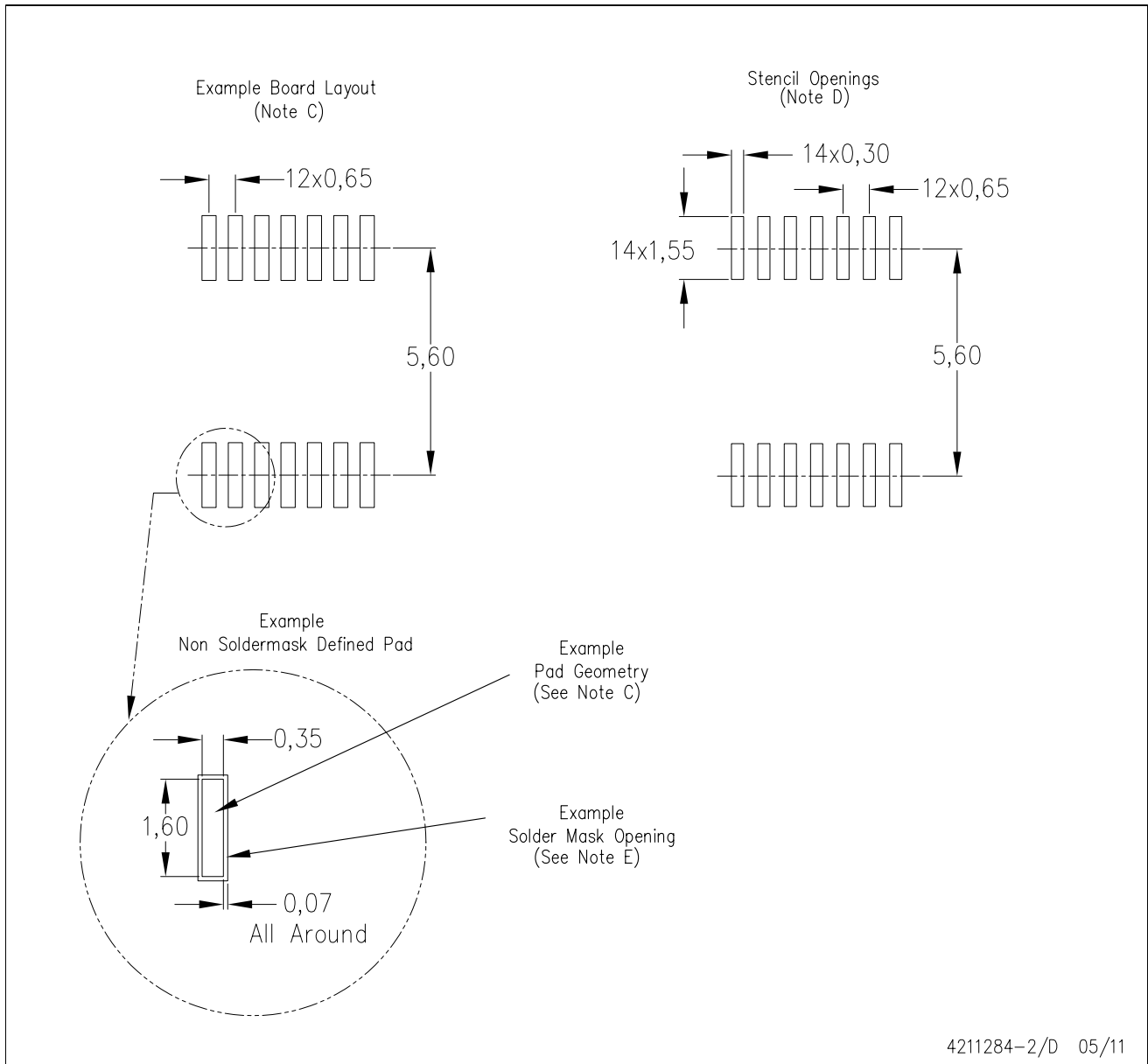
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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